What is claimed is:

[Claim 1] 1. A resistor structure comprising:

a substrate;

a semiconductor layer positioned on the substrate;

a salicide block positioned on portions of the surface of the semiconductor layer; and

at least a salicide layer positioned on the portions of the surface of the semiconductor layer adjacent to the salicide block;

wherein the semiconductor layer comprises a predetermined region overlapping the salicide layer, the junction between the salicide layer and the salicide block, and the portions of the salicide block adjacent to the junction between the salicide layer and the salicide block, and the semiconductor layer has a higher doping concentration within the predetermined region than in the other regions.

[Claim 2] 2. The resistor structure of claim 1 wherein the predetermined region is located at either end of the semiconductor layer.

[Claim 3] 3. The resistor structure of claim 1 further comprising:

an inter layer dielectric positioned on the substrate, the inter layer dielectric comprising at least a contact hole connecting to the salicide layer; and

at least a conductive layer positioned on portions of the surface of the inter layer dielectric and within the contact hole.

[Claim 4] 4. The resistor structure of claim 1 further comprising an ion implantation well positioned underneath the semiconductor layer.

[Claim 5] 5. The resistor structure of claim 1 wherein the semiconductor layer comprises a polysilicon layer.

[Claim 6] 6. The resistor structure of claim 5 further comprising a dielectric layer positioned underneath the semiconductor layer.

[Claim 7] 7. A resistor structure comprising:

a substrate; and

a semiconductor layer positioned on the substrate, the semiconductor layer comprising at least a high resistance region and a low resistance region;

wherein the semiconductor layer comprises a predetermined region overlapping the low resistance region, the junction between the low resistance region and the high resistance region, and the portions of the high resistance region adjacent to the junction between the low resistance region and the high resistance region, and the semiconductor layer has a higher doping concentration within the predetermined region than in the other regions.

[Claim 8] 8. The resistor structure of claim 7 further comprising a salicide block positioned on the portions of the semiconductor layer within the high resistance region.

[Claim 9] 9. The resistor structure of claim 8 further comprising a salicide layer positioned on the portions of the semiconductor layer within the low resistance region.

[Claim 10] 10. The resistor structure of claim 9 wherein the predetermined region overlaps the salicide layer, the junction between the salicide layer and

the salicide block, and the portions of the salicide block adjacent to the junction between the salicide layer and the salicide block.

[Claim 11] 11. The resistor structure of claim 7 wherein the predetermined region is located at either end of the semiconductor layer.

[Claim 12] 12. The resistor structure of claim 7 further comprising:

an inter layer dielectric positioned on the substrate, the inter layer dielectric comprising at least a contact hole connecting to the portions of the semiconductor layer within the low resistance region; and

at least a conductive layer positioned on portions of the surface of the inter layer dielectric and within the contact hole.

[Claim 13] 13. The resistor structure of claim 7 further comprising an ion implantation well positioned underneath the semiconductor layer.

[Claim 14] 14. The resistor structure of claim 7 wherein the semiconductor layer comprises a polysilicon layer.

[Claim 15] 15. The resistor structure of claim 14 further comprising a dielectric layer positioned underneath the semiconductor layer.

[Claim 16] 16. A method of manufacturing a resistor comprising:

providing a substrate;

forming a semiconductor layer on the substrate, the semiconductor layer comprising at least a high resistance region and a low resistance region;

performing a first ion implantation process to the entire surface of the semiconductor layer; and

performing a second ion implantation process to the portions of the semiconductor layer within a predetermined region, the semiconductor layer having a higher doping concentration within the predetermined region than in the other regions;

wherein the predetermined region overlaps the low resistance region, the junction between the low resistance region and the high resistance region, and the portions of the high resistance region adjacent to the junction between the low resistance region and the high resistance region.

[Claim 17] 17. The method of claim 16 further comprising:

forming a salicide block on the portions of the semiconductor layer within the high resistance region; and

forming a salicide layer on the portions of the semiconductor layer within the low resistance region.

[Claim 18] 18. The method of claim 17 wherein the predetermined region overlaps the salicide layer, the junction between the salicide layer and the salicide block, and the portions of the salicide block adjacent to the junction between the salicide layer and the salicide block.

[Claim 19] 19. The method of claim 16 further comprising:

forming an inter layer dielectric on the substrate, the inter layer dielectric comprising at least a contact hole connecting to the portions of the semiconductor layer within the low resistance region; and

forming a conductive layer on portions of the surface of the inter layer dielectric and within the contact hole.

[Claim 20] 20. The method of claim 16 wherein the first ion implantation process and the second ion implantation process use the same type of dopants to implant the semiconductor layer.